REMARKS

Claims 1-12 and 15-22 remain in the application. Claims 1-3, 5, 12, 15, 18 and 19 have been amended. Claims 13 and 14 have been cancelled. Applicants respectfully request allowance of each of pending claims 1-12 and 15-22.

Allowable Subject Matter

Claims 7, 14 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 is now rewritten as the currently-amended independent claim 12 including all of the limitations of its original, base claim 12 and intervening claim 13. As such, the independent claim 12 is now in condition of allowance.

Rejections under 35 U.S.C. §112

Claims 3-6 and 15 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

In claim 3, the language "a first NMOS transistor directly coupled to the high operating voltage" has been amended to "a first NMOS transistor coupled to an output node of the structure." This amended langue is shown in the drawings of the

application. For example, the first NMOS transistor can be the NMOS transistor 208 coupled to the output node OUT in FIG. 2A.

In claim 5, the language "a first PMOS transistor directly coupled to the low voltage" has been amended to "a first PMOS transistor coupled to an output node of the structure." This amended langue is shown in the drawings of the application. For example, the first PMOS transistor can be the PMOS transistor 206 coupled to the output node OUT in FIG. 2A.

Claims 4 and 6 are definite as they now depend on the amended claims 3 and 5, respectively.

With respect to claim 15, the language "the input signal" is supported by an antecedent basis "an input signal" in its base claim 12. Thus, claim 15 is definite.

Rejections under 35 U.S.C. §102

Claims 1-6, 8, 10, 12-13, 15-21 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,370,071 to Lall et al. (hereinafter referred to as "Lall").

The independent claim 1 of the present invention is directed to a cascode device structure having one or more transistors of a same type connected in series and being operable with a normal operating voltage and a high operating voltage. One or more control voltages are controllably coupled to the gates of the transistors, wherein at least one of the control voltages coupled to the gate of at least one transistor is raised to a medium voltage level that is substantially higher than a normal operating voltage and **substantially lower** than the high operating voltage.

The office action dated October 14, 2005 provides that the signal hvb in FIG. 4 of Lall is comparable to the control voltage of the claimed invention (see, lines 19-20, page 3). The Examiner asserts "[t]he voltage at hvb will be equal to Vpp minus the resistive loss from the resistive path P1, P3, thus, the limitation 'substantially ... lower than the high operating voltage' is clearly met as recited in claims 1 and 18" (see, from line 20, page 8 to line 1, page 9). However, Applicants respectfully disagree with the assertion.

The control voltage of the claimed invention is raised to a medium voltage level that is **substantially lower** than the high operating voltage. The ordinary and customary meaning of a term may be evidenced by dictionaries. Texas Digital System, Inc. v, Telegenix, Inc., 308 F.3d 1193, 1202 (Fed. Cir. 2002). The term "substantial" means "large enough in amount or number to be noticeable or to have an important effect." "Substantial," Def. 1, Longman Dictionary of Contemporary English, 3rd ed., 1995. "Substantially" means "very much." "Substantially," Def. 2, Id. As such, the claim language compels a reading that the difference between the medium voltage and the high operating voltage is very much and noticeable.

While the voltage at hvb is equal to Vpp minus the resistive loss from the resistive paths P1 and P3, the resistive loss is negligible. A PMOS transistor is almost perfect for passing "1" signals. Weste, Neil and Kamran Eshraghian, Principles of CMOS VLSI Design: A System Perspective, Massachusetts: Addison-Wesley, 1994, pp. 8 (hereto attached as "Exhibit 1"). Thus, it is understood by those skilled in the art that the resistive loss resulted from Vpp passing through the PMOS transistors P1 and P3 is negligible. This conclusion is further supported by Lall, which provides that when

signal En is low, the signal hvb is at Vpp (see, lines 29-33, col. 4). Thus, hvb cannot be **substantially lower** than Vpp.

As such, the independent claim 1 is not anticipated by Lall under section 102. Accordingly, claims 2-6, 8 and 10 that depend on claim 1 are patentable over Lall as well.

For the same reasons discussed above, claim 2 that discloses the medium voltage level being closer to one half of the high operating voltage than to the high operating voltage is specifically patentable over Lall.

As discussed above, the independent claim 12 includes allowable subject matters and is in condition of allowance. Thus, claims 15-17 that depend on claim 12 are in condition of allowance as well.

For the same reasons discussed above, the independent claim 18 is not anticipated by Lall under section 102. Accordingly, claims 19-21 that depend on claim 18 are patentable over Lall as well.

Rejections under 35 U.S.C. §103

Claims 9 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lall. As discussed above, claims 9 and 11 depend on the independent claim 1 that is patentable over Lall. Thus, they are accordingly patentable over Lall under section 103.

CONCLUSION

Applicants have made an earnest attempt to place this application in an allowable form. In view of the foregoing remarks, it is respectfully submitted that the pending claims are drawn to novel subject matters, patentably distinguishable over the prior art of record. The Examiner is therefore, respectfully requested to reconsider and withdraw the outstanding rejections.

Should the Examiner deem that any further clarification is desirable, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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